CLAIMS

1. A channel assignment process for a switch arrangement, the switch arrangement being arranged to perform the switching of traffic in both the space and time domains, the process comprising:

receiving traffic along a number of ingress subelements of the switch;

for each ingress aggregation comprising a subset of said plurality of ingress subelements, aggregating one or more time-slots of the ingress subelements comprising said ingress aggregation to form one or more aggregated time-space channels;

assigning one or more inner time-space channels available through at least one inner time-shared spatial switching stage of the switch arrangement to each aggregated time-space channel; and

assigning a plurality of end-to-end time-space channels from the plurality of ingress subelements to a plurality of egress subelements through the switch arrangement after said aggregated channels have been assigned through said at least one inner time-shared spatial switching stage.

2. A channel assignment process as claimed in claim 1, wherein each ingress aggregation further comprises a one or more switching stages forming a switching sub-structure of the switch arrangement.

3. A channel assignment process as claimed in claim 1 or 2, wherein said switch arrangement further comprises a plurality of egress aggregations, each egress aggregation comprising a subset of the egress subelements of the switch arrangement and one or more switching stages forming a switching sub-structure of the switch arrangement, wherein for each egress aggregation, one or more time-slots of the egress subelements are aggregated to form one or more aggregated time-space channels.

4. A channel assignment process as claimed in either claim 2 or claim 3, wherein at least one switching stage comprises a time-domain switching stage.

5. A channel assignment process as claimed in any one of claims 3 or 4, wherein in said step of assigning a plurality of end-to-end channels, traffic received at an

ingress subelement is assigned to an end-to-end channel comprising: at least one channel through an ingress aggregation; at least one channel through each of the at least one inner time-shared spatial switching stages of the switch arrangement; and at least one channel through an egress aggregation.

6. A channel assignment process for a switch arrangement as claimed in any preceding claim, wherein the number of time-space inner channels provided by the logical switches of each of said at least one inner time-shared spatial switching stage of the switch arrangement to each ingress aggregation is equal to at least the number of time-slots that each ingress subelement switches end to end through the switch arrangement multiplied by the number of ingress subelements which form an ingress aggregation.

7. A channel assignment process as claimed in any preceding claim, in which the channel assignment process is implemented as a frame-based channel assignment process.

8. A channel assignment process as claimed in any preceding claim, in which said process is further iteratively performed within each ingress aggregation to determine a plurality of end-to-end channels through said ingress aggregation, wherein said inner channels comprise time-space channels provided by the logical switches of at least one inner time-shared spatial switching stage of the ingress aggregation element.

9. A channel assignment process as claimed in any one of claims 3 to 8, in which said process is further iteratively performed within each egress aggregation to determine a plurality of end-to-end channels through each said egress aggregation element, wherein said inner channels comprise time-space channels provided by the logical switches of at least one inner time-shared spatial switching stage of the egress aggregation element.

10. A channel assignment process as claimed in any one preceding claim, in which the step of assigning inner time-space channels available through at least one inner time-shared spatial switching stage of the switch arrangement to said plurality of aggregated time-space channels is implemented using N processors, where N is the number of aggregations of ingress or egress elements of the switch arrangement.

11. A channel assignment process as claimed in any preceding claim, wherein each ingress subelement of the switch arrangement is associated with a plurality of processors arranged to operate in parallel with each other, each processor finding a number of available channels between an ingress subelement and a switch in the final switching stage of an ingress aggregation, wherein the channels within the ingress aggregation element are found by sequential inspection of the status of channels within the ingress aggregation element.

12. A channel assignment process as claimed in any preceding claim, wherein each egress subelement of the switch arrangement is associated with a plurality of processors arranged to operate in parallel with each other, each processor finding a number of available channels between a switch in the first switching stage of an egress aggregation and an egress subelement of the switch arrangement, wherein the channels within the egress aggregation element are found by sequential inspection of the status of channels within the egress aggregation element.

13. A channel assignment process as claimed in any preceding claim, wherein each ingress aggregation of the switch arrangement is provided with one or more processors arranged to operate in parallel with the processors of the other ingress aggregations of the switch arrangement, each processor finding the required number of available aggregated channels between an ingress aggregation and an egress aggregation via the a switch in the final switching stage of an ingress aggregation, wherein the channels are found by sequential inspection.

14. A channel assignment process as claimed in any preceding claim, wherein each ingress aggregation of the switch arrangement is associated with a plurality of processors arranged to operate in parallel with each other, each processor finding a number of available aggregated channels between an ingress aggregation and an egress aggregation via the inner time-shared spatial switching stage of the switch arrangement, wherein the channels are found by sequential inspection of the status of channels from the ingress aggregation and to the egress aggregation.

15. A channel assignment process as claimed in any preceding claim, in which each ingress subelement is associated with n separate processors to perform sequential searching for available channels, each processor searching sequentially

through their channels in parallel with each other; the channel assignment process further comprising the steps of:

each processor counting the number of free channels it determines are available;

a processor sequentially adding the counts from each individual processor until the sum reaches or exceeds the required number of channels or the summation is completed.

16. A channel assignment process as claimed in any preceding claim, in which each ingress aggregation is associated with n separate processors to perform sequential searching for available aggregated channels, each processor searching sequentially through their aggregated channels in parallel with each other; the channel assignment process further comprising the steps of:

each processor counting the number of free aggregated channels it determines are available;

a processor sequentially adding the counts from each individual processor until the sum reaches or exceeds the required number of aggregated channels or the summation is completed.

17. A channel assignment process as claimed in any preceding claim, in which each ingress subelement is associated with n separate processors to perform sequential searching for available channels, each processor searching sequentially through their channels in parallel with each other; the channel assignment process further comprising the steps of:

each processor counting the number of free channels it determines are available; and

a processor or processors adding the summations from the n processors in parallel.

18. A channel assignment process as claimed in any preceding claim, in which each ingress aggregation is associated with n separate processors to perform sequential searching for available aggregated channels, each processor searching sequentially through their aggregated channels in parallel with each other; the channel assignment process further comprising the steps of:

each processor counting the number of free aggregated channels it

determines are available; and

a processor or processors adding the summations from the n processors in parallel.

19. A channel assignment process as claimed in claim 18, wherein the summations from the n processors in parallel are added using multiple stages of a real or a virtual tree of processors.

20. A channel assignment process as claimed in claim 19, wherein the summations from the n processors in parallel are added using $\log_2 n$ stages of a real or a virtual binary tree of processors.

21. A channel assignment process as claimed in one of claims 10 to 20 , wherein the summations from the n processors in parallel are added using multiple stages of a real or a virtual tree of processors.

22. A channel assignment process as claimed in claim 21, wherein the summations from the n processors in parallel are added using $\log_2 n$ stages of a real or a virtual binary tree of processors.

23. A channel assignment process as claimed in any preceding claim, in which a plurality of egress subelements receiving traffic with the same destination are treated as a single a logical entity.

24. A scheduling process for a switch arrangement, the switch arrangement being arranged to perform the switching of traffic in both the space and time domains, the process comprising:

receiving traffic along a number of ingress subelements of the switch;

matching traffic at an ingress subelement of the switch to one or more available egress subelements of the switch; and

assigning channels to matched traffic by performing the steps of:

receiving traffic along a number of ingress subelements of the switch;

aggregating one or more time-slots from each of said plurality of ingress subelements to form a plurality of time-space channels which are aggregated by an aggregation of the said plurality of ingress subelements;

assigning inner time-space channels available through at least one inner time shared spatial switching stage of the switch arrangement to said plurality of aggregated time-space channels; and

assigning a plurality of end-to-end time-space channels from the plurality of ingress subelements to a plurality of egress subelements through the switch arrangement after said aggregated channels have been assigned for switching through the said at least one inner time-shared spatial switching stage.

25. A scheduling process as claimed in claim 24, wherein the number of time-space inner channels provided by the logical switches of each of said at least one inner time-shared spatial switching stage of the switch arrangement to each aggregation element is equal to at least the number of time-slots that each ingress subelement switches end to end through the switch arrangement multiplied by the number of ingress subelements which form an aggregation element.

26. A switching process comprising performing steps in the method of scheduling traffic as claimed in claim 24 or 25, and further comprising the step of:

switching received traffic along said assigned end-to-end channels from the ingress subelements to the egress subelements.

27. A switching process as claimed in claim 26, in which traffic received by an ingress subelement is switched at least once in the time-domain within an ingress aggregation comprising said ingress subelement before being switched spatially by at least one inner time-shared spatial switching stage of the switch arrangement.

28. A switch arrangement arranged to perform the switching of traffic in both the space and time domains, the switch arrangement comprising:

a plurality of ingress subelements;

a plurality of egress subelements;

means to receive traffic along said number of ingress subelements;

means to store said received traffic;

means to aggregate one or more time-slots from each of said plurality of ingress subelements to form a plurality of time-space channels which are aggregated for an ingress aggregation of the said plurality of ingress subelements; and

at least one inner time-shared spatial switching stage, comprising a plurality of logical

switches, wherein said plurality of logical switches are arranged to provide a number of time-space inner channels to each aggregation element which is equal to at least the number of time-slots that each ingress subelement switches end to end through the switch arrangement multiplied by the number of ingress subelements which form an aggregation element; and

switch processor means arranged to switch traffic received by the switch arrangement along a plurality of assigned end-to-end channels from the ingress subelements to the egress subelements.

29. A switch arrangement as claimed in claim 28, in which traffic received by an ingress subelement is switched at least once in the time-domain within an ingress aggregation comprising said ingress subelement before being switched spatially by at least one inner time-shared spatial switching stage of the switch arrangement.

30. A switch arrangement as claimed in claim 28 or 28, further comprising:

means to assign inner time-space channels available through at least one inner time-shared spatial switching stage of the switch arrangement to said plurality of aggregated time-space channels; and

means to assign a plurality of end-to-end time-space channels from the plurality of ingress subelements to a plurality of egress subelements through the switch arrangement after said aggregated channels have been assigned for switching through the said at least one inner time-shared spatial switching stage.

31. A switch arrangement as claimed in any one of claims 28 to 30, wherein the switch is arranged to perform frame-based switching.

32. A switch arrangement as claimed in any one of claims 28 to 31, wherein the switch arrangement is provided with storage means to queue traffic at its subelements.

33. A switch arrangement as claimed in claim 32, wherein said storage means is implemented using virtual output queuing.

34. A switch arrangement as claimed in claim 33, wherein the virtual output queues are implemented in random access memory.

35. A switch arrangement as claimed in any one of claims 28 to 34, wherein the switch arrangement is arranged to switch cells or packets.

36. A switch arrangement as claimed in any one of claims 28 to 35, wherein the switch arrangement includes at least one wavelength switch.

37. A switch arrangement as claimed in any one of claims 28 to 36 wherein the ingress subelements and egress subelements are bi-directional.

38. A switch arrangement as claimed in any one of claims 28 to 37, wherein the number of ingress subelements is not equal to the number of egress subelements.

39. A switch arrangement as claimed in any one of claims 28 to 38, wherein the switch is asymmetric in that the number of ingress aggregations is not equal to the number of egress aggregations.

40. A switch arrangement as claimed in any of claims 28 to 39, wherein the switch arrangement comprises a multi-stage switching structure, wherein within each aggregation of ingress subelements, at least one switching stage is provided.

41. A switch arrangement as claimed in any of claims 28 to 40, wherein the switch arrangement comprises a multi-stage switching structure, wherein within each aggregation of egress subelements, at least one switching stage is provided.

42. A switch arrangement as claimed in any of claims 28 to 41, wherein the switch arrangement comprises a multi-stage switching structure, wherein within each aggregation of ingress subelements, at least one time-switching stage and/or at least one spatial switching stage is provided.

43. A switch arrangement as claimed in any of claims 28 to 42, wherein the switch arrangement comprises a multi-stage switching structure, wherein within each aggregation of egress subelements, at least one time-switching stage and/or at least one spatial switching stage is provided.

44. A switch arrangement as claimed in any of claims 28 to 43, wherein the switch

arrangement comprises a multi-stage switching structure, wherein within at least one ingress aggregation of ingress subelements, a first time-switching stage; a spatial switching stage; and a second time-switching stage are provided.

45 A switch arrangement as claimed in any of claims 28 to 44, wherein the switch arrangement comprises a multi-stage switching structure, wherein within at least one aggregation of egress subelements, a first time-switching stage; a spatial switching stage; and a second time-switching stage are provided.

46. A switch arrangement as claimed in any one of claims 28 to 45, wherein at least one inner spatial switching stage of the switch arrangement comprises one or more space switches which are shared in time between the ingress and egress aggregation elements

47. A switch arrangement as claimed in claim 46, wherein traffic is logically switched by the switch arrangement firstly in a time-switching stage within an aggregation element, secondly by a spatial switching stage within an aggregation element, thirdly by a time-switching stage within an aggregation element, fourthly by a time-shared spatial switching stage of the switch arrangement, fifthly in a time-switching stage within an aggregation element, sixthly by a spatial switching stage within an aggregation element, and finally by a time-switching stage within an aggregation element.

48. A switch arrangement as claimed in claim 47, wherein the switch arrangement comprises a plurality of switching stages forming a permutation of said seven time and spatial switching stages.

49. A switch arrangement as claimed in any one of claims 28 to 48, wherein the arrangement of one or more time-switching stages provided within each ingress aggregation of ingress subelements and/or each egress aggregation of egress subelements implements one or more of the following:

the prevention of data contention at both the ingress subelements and the egress subelements of the switch arrangement;

the correction of the sequencing of data at the egress subelements of the switch arrangement; and

the provision of contiguity of data at the egress subelements of the switch arrangement.

50. A switch arrangement as claimed in any of claims 28 to 49, wherein at least one time-switching stage within is implemented using one or more time-slot interchangers.

51. A switch arrangement as claimed in any of claims 28 to 50, wherein at least one time-switching stage within an ingress aggregation is implemented using one or more virtual output queues implemented in random access memory.

52. A switch arrangement as claimed in any one of claims 28 to 51, wherein the switch arrangement includes parallel processor means arranged to assign said plurality of aggregated time-space channels in parallel to said logical inner channels through the switch arrangement.

53. A switch arrangement as claimed in any one of claims 28 to 52, wherein the switch arrangement includes parallel processor means arranged to assign a plurality of time-space channels in parallel to said logical inner channels through an ingress and/or egress aggregation.

54. A switch arrangement as claimed in claim 52 or 53, wherein the parallel processor means comprises a tree of processors.

55. A switch arrangement as claimed in any one of claims 28 to 54, wherein the switch arrangement is arranged to implement a channel assignment process according to any one of claims 1 to 23.

56. A network comprising one or more switch arrangements as claimed in any one of claims 28 to 55.

57. A suite of one or more computer programs arranged to implement the channel assignment process according to any one of claims 1 to 23.

58. A suite of at least one computer programs arranged to implement the

scheduling process according to any one of claims 24 to 25.

59. A suite of one or more computer programs arranged to implement the switching process according to any one of claims 26 to 27.

60. A suite of at least one computer program as claimed in any one of claims 57 to 59, at least partly arranged to be implemented in hardware.

61. A scheduling process as claimed in claim 24 or 25, including the channel assignment process of any one of claims 1 to 23.

62. A switching process according to any one of claims 26 or 27, in which traffic is scheduled through a switch arrangement according to any one of claims 28 to 55 using a scheduling process as claimed in claim 55.

63. A channel assignment scheme as described herein and with reference to the accompanying drawings.

64. A scheduling scheme as described herein and with reference to the accompanying drawings.

65. A switch arrangement as described herein and with reference to the accompanying drawings.

66. A network as described herein and with reference to the accompanying drawings.

67. A suite of computer programs as described herein an with reference to the accompanying drawings.

68. A channel assignment process for a multi-stage switch arrangement having a plurality of inputs arranged in a plurality of logical associations and a plurality of outputs, wherein time-slotted traffic is received by each logical association of inputs is operated on by one or more switching stages arranged to operate only on traffic provided by the respective logical association of inputs, the channel assignment

process comprising:

for each logical association, aggregating the time-slots carrying traffic from the inputs forming said logical association to form a channel comprising a plurality of logically associated time-slots;

determining a path through a spatial switching stage of the switch arrangement arranged to receive a said channel from each of said logical associations of inputs of the switch arrangement; and

determining a path for each time-slot within each logical association such that a plurality of end-to-end time-space channels are provided for one or more inputs of the switch arrangement to their requested output via said channel through said spatial switching stage of the switch arrangement.

69. A channel assignment process as claimed in claim 68, wherein the outputs of the switch arrangement are logically associated with one or more switching stages, and said step of determining a path for each time-slot within each logical association further comprising determining a path within each logical association of the outputs of the switch arrangement such that said plurality of end-to-end time-space channels are provided.